Einladung zum Vortrag

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Intellectual Property Protection in SoC design

VLSI designs and hardware cores are reused in order to meet the design specifications on time, considering the numerous constraints imposed by nanometer technology. Electronic description of a VLSI design or a hardware core is an intellectual property (IP), and may be infringed upon either in the design house, or the fabrication facility, or at the time of its reuse in a system. This mandates incorporating techniques for intellectual property protection in the VLSI design flow. The IP of a VLSI design, which culminates in fabrication of the integrated circuit, differs from other sources of IPs such as image, text, because in addition to its physical and structural description, it also has a behavioral specification which should remain unaltered by any IP protection technique. IPs at the design level are editable and hence more flexible for reuse yet more vulnerable to misappropriation. Security in activation of chips, especially in embedded systems, is an equally grave issue and has led to the paradigm of design-for-security. This talk aims at presenting the major concerns in IP security and the challenges to implement the countermeasures and retain their effectiveness in the entire life cycle.

Biografie

Susmita Sur-Kolay received the B.Tech degree from Indian Institute of Technology Kharagpur and the Ph.D. degree from Jadavpur University India. She was a Research Assistant at Massachusetts Institute of Technology, post-doctoral fellow at University of Nebraska-Lincoln and Visiting Faculty at Intel Corp., USA. She is presently a Professor in the Advanced Computing and Microelectronics Unit of the Indian Statistical Institute, Kolkata, India. Her research contributions are in the areas of algorithmic CAD for VLSI physical design, fault modeling and testing, IP protection of VLSI design, synthesis of quantum computers, graph algorithms. She has authored several technical papers in international journals and refereed conference proceedings and a chapter in the Handbook on Algorithms for VLSI Physical Design Automation. She was the Technical Program Co-Chair of VLSI Design Conference 2005, VDAT 2007, ISVLSI 2011, and has served on the program committees of several international conferences. She has also been on the editorial board of Proc. of IEE CDT, and an Associate Editor of the IEEE Transactions on VLSI Systems. She is a Distinguished Visitor of IEEE Computer Society(India), Senior Member of IEEE, Member of ACM, IET and VLSI Society of India. Two papers co-authored by her won best paper awards at two international conferences. Among many other awards, she was the recipient of the President of India Gold Medal (summa cum laude) at IIT Kharagpur and IBM Faculty Award.

Dieser Gast wurde von Rolf Drechsler eingeladen.
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